**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Please amend Claims 1, 14, 18, 23, and 24, as follows:

1. (Currently Amended) A circuit for programming a non-volatile memory device having a plurality of memory cells, the circuit including a plurality of driving elements each one for applying a program pulse to a selected memory cell to be programmed, the plurality of driving elements being suitable to be supplied by a power supply unit, and control means for controlling the plurality of driving elements, wherein

the control means includes

means for determining a residual capacity of the power supply unit, and

selecting means for selectively enabling the plurality of driving elements according to the residual capacity of the power supply unit for supplying the programming of the plurality of memory cells.

2. (Original) The circuit according to claim 1, wherein the selecting means enables at least one driving element in succession during a program step of the selected memory cells, the selecting means further including means for disabling each driving element after a predetermined delay from the enabling of the driving element, the delay corresponding to the length of the program pulse, and wherein the control means further includes means for signaling a completion of the program step when all of the driving elements of the enabled at least one driving element have been disabled.

3. (Original) The circuit according to claim 2, wherein the driving elements are grouped into a plurality of subsets each one consisting of a predetermined number of driving elements, the selecting means including means for providing an enabling signal when the power supply unit is in a condition to supply the driving elements of a further subset.

4. (Original) The circuit according to claim 3, wherein the selecting means further includes means responsive to the enabling signal for individually enabling the subsets in succession.

5. (Original) The circuit according to claim 3, wherein the selecting means further includes means responsive to a first enabling signal at the beginning of the program step for enabling a predetermined plurality of subsets, and means responsive to each next enabling signal for individually enabling the remaining subsets in succession.

6. (Original) The circuit according to claim 4, wherein the selecting means further includes means for providing a disabling signal after the predetermined delay from the provision of the enabling signal, means responsive to the disabling signal for disabling the subset enabled by the corresponding enabling signal, and means for providing a signal indicative of the completion of the program step in response to the disabling signal corresponding to a last one of the subsets.

7. (Original) The circuit according to claim 1, wherein the driving elements are grouped into a plurality of subsets each one consisting of a predetermined number of driving elements, the selecting means including means for providing an enabling signal when the power supply unit is in a condition to supply the driving elements of a further subset.

8. (Original) The circuit according to claim 7, wherein the selecting means further includes means responsive to the enabling signal for individually enabling the subsets in succession.

9. (Original) The circuit according to claim 7, wherein the selecting means further includes means responsive to a first enabling signal at the beginning of the program step for enabling a predetermined plurality of subsets, and means responsive to each next enabling signal for individually enabling the remaining subsets in succession.

10. (Original) The circuit according to claim 8, wherein the selecting means further includes means for providing a disabling signal after the predetermined delay from the provision of the enabling signal, means responsive to the disabling signal for disabling the subset enabled by the corresponding enabling signal, and means for providing a signal indicative of the completion of the program step in response to the disabling signal corresponding to a last one of the subsets.

11. (Original) The circuit according to claim 7, wherein the selecting means further includes means responsive to the enabling signal for enabling at most the predetermined number of driving elements selected only among the driving elements associated with memory cells to be programmed.

12. (Original) The circuit according to claim 11, wherein the selecting means includes a logic block for each driving element, the logic blocks being grouped into a plurality of further subsets corresponding to the subsets of the driving elements, each logic block including means for storing an indication of whether the corresponding driving element has been enabled, means for enabling the corresponding driving element in response to the enabling signal when the corresponding memory cell is to be programmed and the corresponding driving element has not been enabled, and means for transmitting the enabling signal to a corresponding logic block of a next further subset otherwise.

13. (Original) The circuit according to claim 12, wherein the selecting means further includes means for providing a disabling signal after the predetermined delay from the provision of the enabling signal, each logic block further including means for storing an indication of whether the corresponding driving element has been disabled, means for disabling the corresponding driving element in response to the disabling signal when the corresponding memory cell is to be programmed and the corresponding driving element has not been disabled, and means for transmitting the disabling signal to the corresponding logic block of the next further subset otherwise, and wherein the selecting means further includes means for providing a signal indicative of the completion of the program step in response to the disabling signal transmitted by all the logic blocks of a last further subset.

14. (Currently Amended) A non-volatile memory device comprises:

a plurality of memory cells; and

a circuit, electrically coupled to the plurality of memory cells, for programming the memory cells of the non-volatile memory device, the circuit including a plurality of driving elements each one for applying a program pulse to a selected memory cell of the plurality of memory cells for programming the selected memory cell, the plurality of driving elements being suitable to be supplied by a power supply unit, and control means for controlling the plurality of driving elements, wherein

the control means includes

means for determining a residual capacity of the power supply unit, and

selecting means for selectively enabling the plurality of driving elements according to the residual capacity of the power supply unit for supplying the programming of the plurality of memory cells.

15. (Original) The non-volatile memory device according to claim 14, wherein the driving elements are grouped into a plurality of subsets each one consisting of a predetermined number of driving elements, the selecting means including means for providing an enabling signal when the power supply unit is in a condition to supply the driving elements of a further subset.

16. (Original) The non-volatile memory device according to claim 15, wherein the selecting means further includes means responsive to the enabling signal for individually enabling the subsets in succession.

17. (Original) The non-volatile memory device according to claim 14, wherein the selecting means enables at least one driving element in succession during a program step of the selected memory cells, the selecting means further including means for disabling each driving element after a predetermined delay from the enabling of the driving element, the delay corresponding to the length of the program pulse, and wherein the control means further includes means for signaling a completion of the program step when all driving elements of the enabled at least one driving element have been disabled.

18. (Original) The circuit according to claim 17, wherein the driving elements are grouped into a plurality of subsets each one consisting of a predetermined number of driving elements, the selecting means including means for providing an enabling signal when the power supply unit is in a condition to supply the driving elements of a further subset.

19. (Currently Amended) A method of programming a non-volatile memory device including a plurality of memory cells and a plurality of driving elements each one for applying a program pulse to a selected memory cell to be programmed, the method including the steps of:

supplying the plurality of driving elements by a power supply unit,

determining a residual capacity of the power supply unit; ~~unit,~~ and

selectively enabling the plurality of driving elements according to the residual capacity of the power supply unit for supplying the programming of the plurality of memory cells.

20. (Original) The method of claim 19, wherein the driving elements are grouped into a plurality of subsets each one consisting of a predetermined number of driving elements, the method further comprising:

providing an enabling signal when the power supply unit is in a condition to supply the driving elements of a further subset.

21. (Original) The method of claim 20, further comprising:

in response to the enabling signal, individually enabling the subsets in succession.

22. (Original) The method of claim 19, wherein the selectively enabling step enables at least one driving element in succession during a program step of at least one selected memory cell, and further comprising the steps of:

disabling each driving element of the at least one driving element after a predetermined delay from the enabling of the respective driving element, the delay corresponding to the length of a program pulse, and

signaling a completion of a program step when all driving elements of the enabled at least one driving element have been disabled.

23. (Currently Amended) An integrated circuit comprising:

a circuit supporting substrate;

a plurality of memory cells; and

a circuit, at least a portion being disposed on the circuit supporting substrate and being electrically coupled to the plurality of memory cells, for programming the memory cells, the circuit including a plurality of driving elements each one for applying a program pulse to a selected memory cell of the plurality of memory cells for programming the selected memory cell, the plurality of driving elements being suitable to be supplied by a power supply unit, and control means for controlling the plurality of driving elements, wherein

the control means includes

means for determining a residual capacity of the power supply unit, and

selecting means for selectively enabling the plurality of driving elements according to the residual capacity of the power supply unit for supplying the programming of the plurality of memory cells.

24. (Currently Amended) A computer system comprising:

a plurality of integrated circuits, each comprising:

a circuit supporting substrate;

a plurality of memory cells; and

a circuit, at least a portion being disposed on the circuit supporting substrate and being electrically coupled to the plurality of memory cells, for programming the memory cells, the circuit including a plurality of driving elements each one for applying a program pulse to a selected memory cell of the plurality of memory cells for programming the selected memory cell, the plurality of driving elements being suitable to be supplied by a power supply unit, and control means for controlling the plurality of driving elements, wherein

the control means includes

means for determining a residual capacity of the power supply unit, and

selecting means for selectively enabling the plurality of driving elements according to the residual capacity of the power supply unit for supplying the programming of the plurality of memory cells.